WHAT IS CLAIMED IS:

1. A solid-state imaging device, comprising:

a plurality of pixel cells arranged on a semiconductor substrate; and

a driving unit that is provided for driving the plurality of pixel cells,

wherein each of the plurality of pixel cells comprises:

a photodiode that converts incident light into a signal charge and stores the signal charge;

a transfer transistor that is provided for reading out the signal charge stored in the photodiode; and

a potential smoothing unit that is formed so as to allow a potential from the photodiode to the transfer transistor to change smoothly.

2. The solid-state imaging device according to claim 1,

wherein the transfer transistor has a gate electrode formed on the semiconductor substrate, and

the potential smoothing unit comprises at least two diffusion layers formed in the semiconductor substrate, each of the diffusion layers having a different depth from a surface of the semiconductor substrate.

3. The solid-state imaging device according to claim 2, wherein the at least two diffusion layers are formed below the gate electrode provided in the transfer transistor.

4. The solid-state imaging device according to claim 1,

wherein the potential smoothing unit comprises a first pocket dissipation-diffusion layer and a second pocket dissipation-diffusion layer,

wherein the first pocket dissipation-diffusion layer is formed for dissipating a first pocket in which the potential from the photodiode to the transfer transistor plunges and the second pocket dissipation-diffusion layer is formed for dissipating a second pocket in which the potential plunges on a side of the transfer transistor with reference to the first pocket.

5. The solid-state imaging device according to claim 4, wherein the first pocket dissipation-diffusion layer is formed at a position deeper than the second pocket dissipation-diffusion layer.

6. The solid-state imaging device according to claim 4, wherein the

potential smoothing unit further comprises a barrier dissipation–diffusion layer that is formed for dissipating a barrier of the potential occurring between the first pocket and the second pocket.

7. The solid–state imaging device according to claim 6,

wherein the first pocket dissipation–diffusion layer is formed at a position deeper than the barrier dissipation–diffusion layer, and

the barrier dissipation–diffusion layer is formed at a position deeper than the second pocket dissipation–diffusion layer.

8. The solid–state imaging device according to claim 6, wherein the first pocket dissipation–diffusion layer, the barrier dissipation–diffusion layer and the second pocket dissipation–diffusion layer are composed of p–type impurity diffusion layers.

9. The solid–state imaging device according to claim 6,

wherein the first pocket dissipation–diffusion layer and the second pocket dissipation–diffusion layer are composed of p–type impurity diffusion layers, and

the barrier dissipation–diffusion layer is composed of a n–type impurity diffusion layer.

10. The solid–state imaging device according to claim 6,

wherein an end of the first pocket dissipation–diffusion layer on a side of the photodiode is closer to the photodiode than to an end of the barrier dissipation–diffusion layer on a side of the photodiode, and

the end of the barrier dissipation–diffusion layer on the side of the photodiode is closer to the photodiode than to an end of the second pocket dissipation–diffusion layer on a side of the photodiode.

11. The solid–state imaging device according to claim 4, wherein the first pocket dissipation–diffusion layer is formed at a position of about 0.7 μm in depth from a surface of the semiconductor substrate.

12. The solid–state imaging device according to claim 4, wherein the second pocket dissipation–diffusion layer is formed at a position shallower than a depth of about 0.2 μm from a surface of the semiconductor substrate.

13. The solid–state imaging device according to claim 6, wherein the barrier dissipation–diffusion layer is formed at a position of about 0.4 μm in depth from a surface of the semiconductor substrate.

14. The solid–state imaging device according to claim 1,
wherein the photodiode comprises:
a shallow p–type photodiode diffusion layer formed in the semiconductor substrate; and
a deep photodiode diffusion layer that is formed below the shallow p–type photodiode diffusion layer so as to be exposed from a portion of a surface of the semiconductor substrate that is located between the shallow p–type photodiode diffusion layer and the transfer transistor.

15. The solid–state imaging device according to claim 1,
wherein each of the plurality of pixel cells further comprises:
a floating diffusion layer that is formed for converting the signal charge read out from the photodiode by the transfer transistor into a voltage;
a reset transistor that is formed for resetting the signal charge stored in the floating diffusion layer; and
a source follower that is provided for amplifying a change in the voltage that is converted by the floating diffusion layer or converting an impedance.

16. The solid–state imaging device according to claim 1, wherein the plurality of pixel cells are formed in a matrix form on the semiconductor substrate.

17. The solid–state imaging device according to claim 16,
wherein the driving unit comprises:
a vertical driving circuit for driving the plurality of pixel cells along a row direction; and
a horizontal driving circuit for driving the plurality of pixel cells along a column direction.

18. A method for manufacturing the solid–state imaging device

according to claim 1, comprising the steps of:

forming the potential smoothing unit for allowing a potential from the photodiode to the transfer transistor to change smoothly;

forming the photodiode for converting the incident light into the signal charge and storing the signal charge, which is conducted after the step of forming the potential smoothing unit; and

forming the transfer transistor for reading out the signal charge stored in the photodiode, which is conducted after the step of forming the photodiode,

wherein, in the step of forming the potential smoothing unit, an impurity is implanted at a region between a region where the photodiode is to be formed and a region where the transfer transistor is to be formed, the injection being carried out using three different levels of energy.

19. The method for manufacturing a solid-state imaging device according to claim 18, wherein the impurity implanted in the step of forming the potential smoothing unit comprises an ion having a same conductivity type as that of the semiconductor substrate.

20. The method for manufacturing a solid-state imaging device according to claim 19,

wherein the step of forming the potential smoothing unit comprises the steps of:

forming a first pocket dissipation-diffusion layer for dissipating a first pocket in which the potential from the photodiode to the transfer transistor plunges;

forming a barrier dissipation-diffusion layer on the first pocket dissipation-diffusion layer, the barrier dissipation-diffusion layer being formed for dissipating a barrier of the potential occurring between the first pocket and a second pocket; and

forming a second pocket dissipation-diffusion layer on the barrier dissipation-diffusion layer, the second pocket dissipation-diffusion layer being formed for dissipating the second pocket in which the potential plunges on a side of the transfer transistor with reference to the first pocket.

21. The method for manufacturing a solid-state imaging device according to claim 20,

wherein, in the first pocket dissipation–diffusion layer formation step, the impurity is implanted using a first energy so as to form the first pocket dissipation–diffusion layer,

in the barrier dissipation–diffusion layer formation step, the impurity is implanted using a second energy smaller than the first energy so as to form the barrier dissipation–diffusion layer, and

in the second pocket dissipation–diffusion layer formation step, the impurity is implanted using a third energy smaller than the second energy so as to form the second pocket dissipation–diffusion layer.

22. The method for manufacturing a solid–state imaging device according to claim 20,

wherein, in the first pocket dissipation–diffusion layer formation step, the impurity is implanted under conditions of an acceleration voltage of 300 keV and a dose of $4.0 \times 10^{12}/cm^2$,

in the barrier dissipation–diffusion layer formation step, the impurity is implanted under conditions of an acceleration voltage of 100 keV and a dose of $8.0 \times 10^{11}/cm^2$, and

in the second pocket dissipation–diffusion layer formation step, the impurity is implanted under conditions of an acceleration voltage of 10 keV and a dose of $4.0 \times 10^{11}/cm^2$.

23. The method for manufacturing a solid–state imaging device according to claim 18, wherein the impurity is a boron ion.

24. An interline transfer CCD image sensor, comprising:

a plurality of pixel cells arranged in a matrix form on a semiconductor substrate; and

a driving unit that is provided for driving the plurality of pixel cells,

wherein each of the plurality of pixel cells comprises:

a photodiode that converts incident light into a signal charge and stores the signal charge;

a transfer gate that is provided for reading out the signal charge stored in the photodiode; and

a potential smoothing unit that is formed so as to allow a potential from the photodiode to the transfer gate to change smoothly.

25. The interline transfer CCD image sensor according to claim 24, further comprising vertical transfer CCDs that are arranged at predetermined intervals and along a vertical direction so as to be adjacent to the respective pixel cells that are arranged along the vertical direction, the vertical transfer CCDs being provided for transferring the signal charge read out from the photodiode by the transfer gate along the vertical direction.